

Amendments to the Drawings:

Please amend the drawings to correct errors, as described below. Replacement Sheets for Figs. 5, 7 and 8, are attached hereto in the Appendix.

Fig. 5 – “from 408” should read “from 404”; “to 412” should read “to 413”.

Fig. 7 – LEFT SIDE OF FIGURE: The two arrows originating at the asterisk (*) of entry “p4” and at the asterisk (*) of entry “p17” of table 102 should both point to entry S2 of table 104. Currently, both arrows incorrectly point to entry S1 of table 104.

Fig. 7 – RIGHT SIDE OF FIGURE: The arrow originating at the asterisk (*) of entry “p17” of table 102 should point to entry S2 of table 104. Currently, the arrow incorrectly points to entry S1 of table 104.

Fig. 8 – LEFT SIDE OF FIGURE: The arrow originating at the asterisk (*) of entry “p17” of table 102 should point to entry S2 of table 104. Currently, the arrow incorrectly points to entry S1 of table 104.

Fig. 8 – RIGHT SIDE OF FIGURE: The arrow originating at the asterisk (*) of entry “p17” of table 102 should point to entry S2 of table 104. Currently, the arrow incorrectly points to entry S1 of table 104.

REMARKS and ARGUMENTS

Claims 1-8 and 14-22 stand rejected under 35 U.S.C. 102(b) as being anticipated by Eikemeyer (U.S. Patent No. 6,393,552 B1). Claims 9-13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Eikemeyer in view of Intel Architecture Software Developer's Manual. Claims 9, 10, 14, 16, 17 and 19 have been amended, as have the Specification and the some of the Drawings.

Applicants wish to express their appreciation for the time the Examiner Moll took to discuss Claims 1 and 14 with Shireen Bacon on June 2, 2006. His time and insight were much appreciated.

Objections to the Specification

The Office Action objects that the title of the Application is not descriptive, and suggests an amended title. The title has been amended as suggested in the Office Action. The objection has been overcome.

The Office Action also objects to an alleged typographical error in entry 5 of Table 1. However, such error was not in the Application as filed by Applicants (see, for example, the PAIR copy of the Application as originally filed). Applicants suspect that the typographical error was injected into the Application by the Patent Office during the publication process. In case amendment is nonetheless needed on Applicants' part, the amendment has been outlined above to change the word 'appropnate' to "appropriate". The objections to the Specification have been overcome and should be withdrawn.

Objections to the Claims

The Office Action objects to Claims 9, 14 and 17 for informalities. Claim 9 has been amended, as suggested in the office action, to change “n” to another variable. Applicants have chosen “x”, which is not otherwise used in the claims, as the new variable.

Claim 17 has been amended as suggested in the Office Action to change the dependence from claim 14 to claim 16. The objections to Claims 9 and 17 thus have been overcome and should be withdrawn.

Regarding Claim 14, the Office Action makes multiple objections to the claim. The Office Action indicates that there is insufficient antecedent basis for the term “the destination register” at line 8 of Claim 14. Claim 14 has been amended to provide the antecedent basis in the first element of the claim. Thus, this particular objection to Claim 14 has been overcome.

The Office Action also complains that the wording of Claim 14 is unclear: “[i]t is unclear whether the register can be written in accordance with any access type, or is somehow limited by the specific access types listed.” Applicants have amended Claim 14 to remove the objected claim language. Thus, this particular objection to Claim 14 has been overcome. The objections to Claim 14 should therefore be withdrawn.

Claim rejections - 35 U.S.C. § 102(b)

Claims 1-8 and 14-22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Eikemeyer et al., U.S. Patent No. 6,393,552. However, the prima facie case of anticipation has not been made.

Eikemeyer discloses a method and implementing system in which processor registers are divided into sectors and such sectors are individually renamed. (Eikemeyer, Abstract). Importantly, each of the physical registers in the Eikemeyer register rename file 303 are partitioned into sectors of the same size – 32 bits. (Eikemeyer, Fig. 3). Although Eikemeyer indicates that other sized could be used for the sectors (“smaller sectors are also possible” – Col. 3, Line 49), Eikemeyer discloses that all sectors are the same size, whatever that size happens to be. There is absolutely no teaching, disclosure or suggestion in Eikemeyer that the register file may include different sizes of registers – that is, some registers having a first length and other registers having a second length (“fat” and “skinny” registers).

The Office Action claims that differing lengths of registers, as claimed by Applicants in Claim 1, is taught by Eikemeyer because: “if both status bits are set, the processor renames using the RR1 register (which is 64 bits long); otherwise, it uses RR1A register (which is 32 bits long).” The Office Action admits that registers RR1A and RR1 do share common bits and therefore are not separate registers. This is reinforced by Eikemeyer at Col. 4, lines 14 – 16, which indicate that “the group of registers available for renaming consists of a number of 32-bit registers.” It is also reinforced by Eikemeyer at Col. 3, lines 59 – 61: “[e]ach sector A 309 and B 311 provides an independent 32-bit rename register as shown such as RR1A and RRLB [sic].” There is only one size of register (32-bit) available for renaming. At times, two of these registers are used for renaming for 64-bit registers. Thus, the Eikemeyer rename registers are all the same size; sometimes multiple of them are used for renaming, but this does not change the fact that all the rename registers are the same size.

Instead, Applicants disclose that its first and second rename registers are separate sets of rename registers 104, 106, with each set of registers having a different size. This distinction has been made more clear by the amendment to Claim 1, which recites: “wherein the first and second rename registers are distinct from each other and do not share common bits.” Such limitation is not disclosed, suggested nor taught by Eikemeyer. Claim 1 is allowable for at least this reason. The rejection should therefore be withdrawn and amended Claim 1 should be allowed to issue. In addition, Claims 2 - 13, which depend from Claim 1, are also allowable for at least the foregoing reasons and should be allowed to issue.

Regarding Claim 14, the Office Action has also failed to make out a prima facie case of anticipation. Amended Claim 14 recites “responsive to the current instruction indicates indicating a partial-bit write of only 1 bit position of the MBF.” (Claim 14, in part) Eikemeyer does not disclose, suggest nor teach this limitation.

Eikemeyer does not disclose, suggest or teach that an instruction may indicate that only one bit of an MBF should be written. This is confirmed in the Office Action, which states that “the partial bit write is a 1 sector write of 32 bits (one sector) and the bulk-bit write is a 2-sector write of 64 bits.” A 1 sector write of 32 bits does NOT read on “a partial write of only 1 bit position of the MBE.” A prima facie case of anticipation with regard to Claim 14 has not been made out for at least this reason. The rejection of Claim 14 should be withdrawn, and Claim 14 should be allowed to issue. For at least the foregoing reasons, the rejection of dependent Claims 15 – 22 should also be withdrawn and the claims should be permitted to issue.

Claim Rejections - 35 U.S.C. § 103(a)

Claims 9-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Eikemeyer in view of Intel Architecture Software Developer's manual Volume 2: Instruction Set Reference ("Intel"). However, the prima facie case of obviousness has not been made.

Regarding Claim 9, the Office Action admits that Eikemeyer does not expressly disclose that a selected one of the n bit positions may be accessed individually responsive to a first instruction that indicates the selected bit position nor does it expressly disclose that the rename logic is further to allocate the first physical rename register responsive to the first instruction. Applicants agree.

The Office Action states that these elements are shown in Intel. However, the Office Action does not provide sufficient evidence of motivation to combine the Eikemeyer and Intel references. A prima facie case of anticipation therefore has not been made out with respect to Claim 9.

The motivation for Eikemeyer was to address the register inefficiencies for RISC processors, such as for the PowerPC processor, that were introduced as 32-bit architecture and later extended to 64-bit. "Existing applications written for the 32-bit processors must still run on the 64-bit processors." (Eikemeyer, Col. 2, lines 3 – 24). Full register renaming wastes register space and slows down processor performance for code using 8, 16, or 32 bits of data. Thus, renaming of full 64-bit registers in Eikemeyer

was modified so that the processor could execute more efficiently when using smaller integer values: 8, 16 and 32-bit values. Id.

There is no suggestion or motivation that the Eikemeyer scheme could benefit from allowing access for single bits of a register. Since integer values are not typically represented with a single bit, there is no suggestion or teaching that one of skill in the art would have been motivated to modify the teaching of Eikemeyer to provide one-bit register access.

In addition, Claim 9 depends from Claim 1 (via intervening Claim 8). As is set forth above in the preceding section, Claim 1 includes limitations for which a prima facie case of anticipation has not been made out with respect to Eikemeyer. Thus, neither Eikemeyer or Intel, either alone or in combination, discloses, suggests or teaches every element of Claim 9.

Accordingly, for at least the foregoing reasons the Office Action has not made out a prima facie case of obviousness with respect to Claim 9. The rejection should be withdrawn and Claim 9 should be allowed to issue. In addition, Claims 10 – 13, which depend from Claim 9, are also allowable for at least the foregoing reasons.

Accordingly, Applicants respectfully submit that the applicable rejections have been overcome and must all be withdrawn. Applicants reserve all rights with respect to the application of the doctrine equivalents. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If the Examiner feels that an interview would help to resolve any remaining issues in the case, the Examiner is invited to contact Shireen Bacon of Intel, at (512) 732-3917.

Please charge any shortages and credit any overcharges to our Deposit Account
No. 02-2666.

Respectfully submitted,

Dated: June 2, 2006

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APPENDIX

Replacement Sheet for Fig. 5

Replacement Sheet for Fig. 7

Replacement Sheet for Fig. 8